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Modeling of MMCs With Controlled DC-Side Fault Blocking Capability for DC Protection Studies

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***Abstract*—The fault current characteristics in dc systems depend largely on the response, and hence also the topology, of the ac-dc converters. The presently used ac-dc converter topologies may be categorized into those with controlled or uncontrolled fault blocking capability and those lacking such capability. For the topologies of the former category, generic models of the dc-side fault response have not yet been developed and a characterization of the influence of control and sensor delays is a notable omission. Therefore, to support accurate and comprehensive dc system protection studies, this paper presents three reduced converter models and analyzes the impact of key parameters on the dc-side fault response. The models retain accurate representation of the dc-side current control, but differ in representation of the ac-side and internal current control dynamics, and arm voltage limits. The models were verified against a detailed (full-switched) simulation model for the cases of a full-bridge and a hybrid modular multilevel converter, and validated against experimental data from a lab-scale prototype. The models behave similarly in the absence of arm voltage limits, but only the most detailed of the three retains a high degree of accuracy when these limits are reached.**

***Index Terms*—ac-dc power conversion, current control, HVDC converters, power system protection, short-circuit currents**

NOMENCLATURE

Control

$\boldsymbol{x}$, $\boldsymbol{u}$, $\boldsymbol{w}$	State, control input and disturbance input vector
$\boldsymbol{r}$	Reference input
$\boldsymbol{A}$, $\boldsymbol{B}$, $\boldsymbol{E}$	Continuous-time state, control and disturbance matrix
$\boldsymbol{\Phi}$, $\boldsymbol{\Gamma}$, $\boldsymbol{\mathcal{E}}$	Discrete-time state, control and disturbance matrix
$\boldsymbol{H}$	Discrete-time output matrix
$\boldsymbol{K}$	Proportional gain matrix
$\boldsymbol{L}$	Estimator gain matrix
$\boldsymbol{N}$	Combined state command and proportionality constant matrix
$\boldsymbol{T}_{\mathbf{i}}$, $\boldsymbol{T}_{\mathbf{u}}$	State and control transformation matrix
$\boldsymbol{Q}$, $\boldsymbol{R}$	LQR design state and control weighting matrix
ρ	Current control design parameter
$\boldsymbol{G}_{\mathbf{MMC}}$	MMC transfer function matrix
$\boldsymbol{G}_{\mathbf{E}}$	Estimator transfer function matrix
$\tau_{\mathbf{c}}$, $\tau_{\mathbf{s}}$	Control and sensor delay

Electrical quantities

$v_{\mathbf{u,l}}$	Upper and lower arm inserted voltage
$v_{\mathbf{ac}}$	ac-side phase voltage
$v_{\mathbf{dc}}^{+}$, $v_{\mathbf{dc}}^{-}$	dc-side positive and negative pole-to-ground voltage
$v_{\mathbf{dc}}$	dc-side pole-to-pole voltage
$i_{\mathbf{u,l}}$	Upper and lower arm current
$i_{\mathbf{ac}}$	ac-side current
$i_{\mathbf{dc}}^{+}$, $i_{\mathbf{dc}}^{-}$	dc-side positive and negative pole current
$i_{\mathbf{dc}}$	dc-side current
$L_{\mathbf{arm}}$, $L_{\mathbf{arm}}^{\mathbf{eq}}$	Arm inductance, equivalent
$R_{\mathbf{arm}}$, $R_{\mathbf{arm}}^{\mathbf{eq}}$	Arm resistance, equivalent

Additional notation

$^{\mathbf{dc}}$	Part of matrix, parameter, transfer function or input associated with the dc-side component
$_{\Sigma}$	Sum component
$_{\mathbf{d}}$	Value delayed by τ_{c}
$_{\mathbf{m}}$	Value delayed by τ_{s}
$\bar{\ }$	Saturated value
$\tilde{\ }$	Transformed matrix or variable
$'$	Augmented matrix or variable
$^{\mathbf{ctrl}}$, $^{\mathbf{prt}}$	Variable associated with normal, and fault conditions

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I. INTRODUCTION

Power electronic interfaced dc systems are emerging at all voltage levels of the modern power system. These systems support the need for increased transmission capacity and flexibility in power system operation when dealing with large amounts of renewable energy such as solar power and wind, as e.g. shown in [1]. In the high-voltage system, dc connections have been in use for several decades in the form of High-Voltage Direct Current (HVDC) point-to-point links based on Line Commutated Converter- (LCC) or Voltage Source Converter (VSC)-technology [2]. At present, two multi-terminal VSC HVDC systems have already been built in China, e.g., the project discussed in [3]. Furthermore, research is ongoing towards achieving HVDC, Medium- and Low-Voltage Direct Current (MVDC and LVDC) grids [4]–[6]. These dc systems have radically different characteristics with respect to system control and protection in comparison to existing ac systems.

The ac-dc converters can be roughly classified into three main categories with respect to the dc-side fault response [18]. These categories are non-fault blocking, e.g., two-level [19] or half-bridge modular multilevel converter (MMC) [14], [15], uncontrolled fault blocking (in some cases also referred to

TABLE I
EXISTING AND PROPOSED MMC MODELS FOR DC-SIDE FAULT STUDIES

Model type	Fault Response	Circuit Model	SM Stack Model	Arm Voltage Limit	Control Loops Modeled		
					Arm Bal.	CC	SM Bal.
Full-switching	N/U/C	Three phase	Individual SMs	Dynamic	Y	Y	Y
Arm Equiv.	N [7]/U [8]	Three phase	Thév./Norton Equiv.	Dynamic	Y	Y	Y
Arm-Level Avg.	N [9]–[11]	Three phase	Voltage source/Diode	Dynamic	Y	Y	N
Arm-Level Avg.	U [12]/C [13]	Three phase	Voltage source	Dynamic	Y	Y	N
Equivalent Circuit	N [14], [15]/U [16], [17]	Three phase	Equiv. C/Diode	n/a	N	N	N
Three-phase EMT-type	C	Three phase	Voltage source	**Fixed**	**N**	Y	**N**
DC EMT-type	C	dc-side equiv.	**n/a**	**(dc-side) Fixed**	**N**	Y	**N**
Transfer Function	C	dc-side equiv.	**n/a**	**n/a**	**N**	Y	**N**

N/U/C: Non-/Uncontrolled/Controlled fault blocking

as "dc-side fault ride through"), e.g., MMC with blocking-capable-only submodules [20], [21] or control [16], [17], and controlled fault blocking, e.g., MMC or MMC-like topologies that retain current control during dc-side faults [22], [23]. The converters of the non-fault blocking type are unable to prevent the ac system from contributing to the dc-side fault current, as a path for the fault current exists through the anti-parallel diodes of their power electronic switches. By contrast, the converters of the blocking type possess the capability to prevent the ac system from contributing to the dc-side fault through inserting a voltage which opposes the ac-side voltage in either an uncontrolled or controlled manner, depending on their circuitry. The converters with uncontrolled fault blocking capability typically stop active switching upon detection of a fault, and oppose the ac-side voltage in a passive way. Converters with controlled fault blocking capability remain actively switched while opposing the ac side voltage.

The traditional models of MMCs that also accurately represent the response to dc-side faults have limitations with respect to parametric system studies involving a large number of parameters or involving more than one converter. The full-switching (or submodule-level switched models according to [24]), e.g., up to Type III in [25], are computationally expensive due to the large number of nodes needed to model the submodule stacks. The equivalent modeling method, introduced in [26] and termed Type IV in [25] may increase computational efficiency but nevertheless involves calculation of a large number of variables (i.e., the submodule voltages). The continuous model introduced in [9] can be used in a submodule-level or arm-level averaged model. An MMC model based on the latter representation, although computationally more efficient compared to the full-switching model, nonetheless retains a level of complexity in modeling internal energy balancing controls and calculating the associated internal variables.

The increasing use of dc systems calls for a unified approach towards modeling of ac-dc converters for dc system protection studies. Modeling of the dc-side fault response for converters without or with uncontrolled fault blocking capability have received considerable attention in the literature, e.g., in [8], [10]–[12], [14]–[17], [19], [25], [27], [28] (the latter study focuses on dc-dc converters). For converters without fault blocking capability, the essence to provide correct dc-side fault response is to correctly model the states of initial controlled response (unblocked state) and uncontrolled rectification (blocked state), and the transition in between. In full-switching models, the uncontrolled rectification state is inherently present in the model. In mathematically equivalent submodule or reduced arm representations, such a state has to be manually added by adding a circuit with anti-parallel diodes to provide a path for the fault currents, see, e.g., [7], [9], [10], [14] for details. Converters with uncontrolled fault blocking capability can be treated in a similar fashion whereas in this case the uncontrolled blocked state and the transition to that state must be correctly modeled, as done in [8], [12], [17]. The aforementioned modeling approaches may not be applicable to converters with controlled fault blocking capability, given the essential differences in dc-side fault response. This is so because, for the latter category, there is no need to transition to a blocked state as the converter retains control of its arm currents even during the dc-side fault. In the literature, modeling requirements for dc-side fault or protection studies involving converters with controlled fault blocking capability have not yet been fully assessed.

Recent literature indicates that dc-side fault studies involving converters with controlled fault blocking capability are performed mainly with traditional MMC models such as full-switching or arm-level averaged. For instance, in [29]–[32], important aspects are pointed out related to the dc-side fault response of a full-bridge MMC, but the analysis is restricted to the results of a limited number of fault cases. The results in [29], [31], [32] were obtained using a full-switching simulation model and the main contributions in [31] and [30] were verified using a hardware prototype. In [13], an arm-level averaged model for the Alternate Arm Converter (AAC) was tested for dc-side fault response.

To support accurate and efficient dc-side protection studies involving converters with controlled dc-side fault blocking capability, we have developed three reduced converter models, named three-phase EMT-type, dc EMT-type and transfer function model. The developed models increase computational efficiency and reduce model complexity compared with the state-of-the-art, i.e., full-switching or continuous models retaining converter internal dynamics. The focus of the proposed models is to accurately represent the dc-side system response of the converters to dc-side faults rather than the converter internal dynamics. The key to reducing model complexity is to use an averaged arm representation without dynamic arm voltage limits, such that computationally expensive tasks such as submodule voltage calculation, arm energy or submodule voltage balancing are avoided, as shown in Table I. The main features of the proposed models in correctly modeling the dc-side fault response are the inclusion of discrete-time current control with control and sensor delays, and negative arm voltage limits. To verify the proposed models, we have analyzed the impact of relevant parameters and controls on the converter's response to dc-side faults and we have supported this analysis by experiments using a lab-scale converter prototype.

In this paper, the controlled dc-side fault blocking capability is first discussed in Section II, prior to describing the developed models in Section III. The impact of relevant parameters and the accuracy of the proposed converter models are verified using a detailed model in a simulation environment and a lab-scale converter prototype, of which the outcomes are discussed in Section VI. The main conclusions of this work are stated in Section IV.

II. Controlled DC-side Fault Blocking

Controlled dc-side fault blocking depends on fast current control, which quickly responds to the disturbances introduced by the fault, and on the capability of the converter to inject negative arm voltages. In the following paragraphs, we mainly focus the discussion on these aspects and base ourselves on the MMC equivalent diagrams shown in Fig. 1a, where submodule stacks have been represented as controllable voltage sources. For a more detailed overview of the MMC and its modeling and control, we refer the reader to [20], [24], [25], [33]–[37].

A. Converter Current Control

The converter current control ensures that the external ac and dc system currents as well as the currents in each branch of the converter are made to track as closely as possible to their reference currents, where these reference currents are taken from the outer control loops such as active power and energy balance control, e.g., as shown in [37]. To track these reference currents, the current control generates voltage reference waveforms for each converter arm. The voltage reference waveforms are sent to the low-level control of each arm, where they are converted into signals for the gate drivers of the power electronic switches within the submodules.

Although the analysis can be performed for any control structure, the current control is, in this work, analyzed using state-feedback control. The state-feedback control and the associated state-space analysis provide an elegant way for analyzing the dynamics during dc-side faults. The state-space model of the MMC in continuous time can be expressed in the form (cf. Fig 1a):

$$\dot{\boldsymbol{x}}(t) = \boldsymbol{A}\boldsymbol{x}(t) + \boldsymbol{B}\boldsymbol{u}(t) + \boldsymbol{E}\boldsymbol{w}(t), \tag{1}$$

where

$\boldsymbol{x}(t)$ is the vector of the state variables which contains a set of independent currents associated with the MMC. These independent currents are typically composed of a combination of selected ac and dc external currents, $\boldsymbol{i}_{\mathrm{ac}} = [i_{\mathrm{ac}}^{\mathrm{a}}, i_{\mathrm{ac}}^{\mathrm{b}}, i_{\mathrm{ac}}^{\mathrm{c}}]$ and $\boldsymbol{i}_{\mathrm{dc}} = [i_{\mathrm{dc}}^{+}, i_{\mathrm{dc}}^{-}]$, and ac internal currents in the upper and lower arm $\boldsymbol{i}_{\mathrm{u,l}} = [i_{\mathrm{u}}^{\mathrm{a}}, i_{\mathrm{u}}^{\mathrm{b}}, i_{\mathrm{u}}^{\mathrm{c}}, i_{\mathrm{l}}^{\mathrm{a}}, i_{\mathrm{l}}^{\mathrm{b}}, i_{\mathrm{l}}^{\mathrm{c}}]$.

$\boldsymbol{u}(t)$ is the vector of the control variables, which are the arm voltages $[\upsilon_{\mathrm{u}}^{\mathrm{a}}, \upsilon_{\mathrm{u}}^{\mathrm{b}}, \upsilon_{\mathrm{u}}^{\mathrm{c}}, \upsilon_{\mathrm{l}}^{\mathrm{a}}, \upsilon_{\mathrm{l}}^{\mathrm{b}}, \upsilon_{\mathrm{l}}^{\mathrm{c}}]$.

$\boldsymbol{w}(t)$ is the vector of the disturbance variables, which consist of the ac and dc system voltages $\boldsymbol{\upsilon}_{\mathrm{ac}} = [\upsilon_{\mathrm{ac}}^{\mathrm{a}}, \upsilon_{\mathrm{ac}}^{\mathrm{b}}, \upsilon_{\mathrm{ac}}^{\mathrm{c}}]$ and $\boldsymbol{\upsilon}_{\mathrm{dc}} = [\upsilon_{\mathrm{dc}}^{+}, \upsilon_{\mathrm{dc}}^{-}]$.

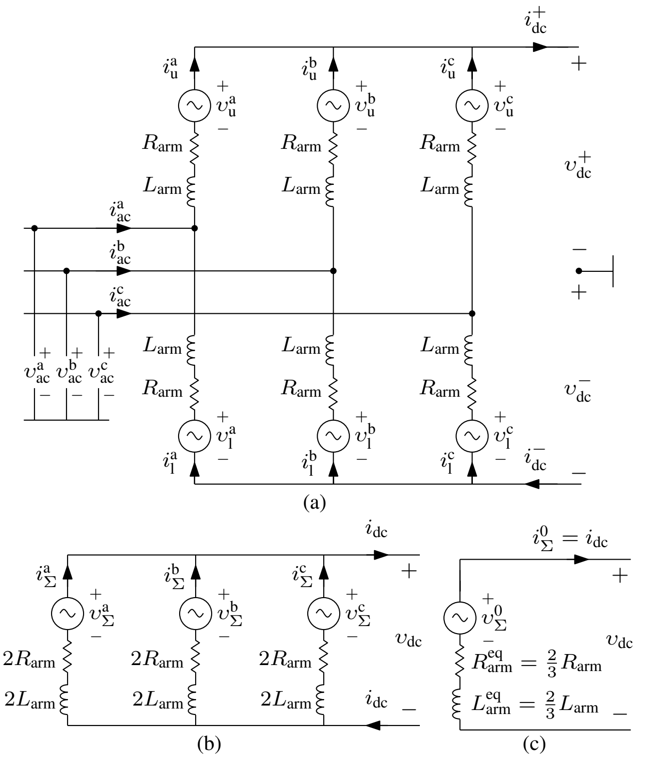


Fig. 1. MMC equivalent circuit diagram (a) and derivation to sum components (b) and dc component (c) equivalent circuit diagrams.

When applying time-invariant transforms to the state and control variables, with the respective transforms for each given by $\boldsymbol{T}_{\mathrm{i}}$ and $\boldsymbol{T}_{\mathrm{u}}$, a decoupled system equation is obtained:

$$\dot{\tilde{\boldsymbol{x}}}(t) = \underbrace{\boldsymbol{T}_{\mathrm{i}}^{-1}\boldsymbol{A}\boldsymbol{T}_{\mathrm{i}}}_{\tilde{\boldsymbol{A}}}\tilde{\boldsymbol{x}}(t) + \underbrace{\boldsymbol{T}_{\mathrm{i}}^{-1}\boldsymbol{B}\boldsymbol{T}_{\mathrm{u}}}_{\tilde{\boldsymbol{B}}}\tilde{\boldsymbol{u}}(t) + \underbrace{\boldsymbol{T}_{\mathrm{i}}^{-1}\boldsymbol{E}}_{\tilde{\boldsymbol{E}}}\boldsymbol{w}(t), \tag{2}$$

in which $\boldsymbol{x}(t) = \boldsymbol{T}_{\mathrm{i}}\tilde{\boldsymbol{x}}(t)$ and $\boldsymbol{u}(t) = \boldsymbol{T}_{\mathrm{u}}\tilde{\boldsymbol{u}}(t)$ and $\tilde{\boldsymbol{A}}$, $\tilde{\boldsymbol{B}}$, and $\tilde{\boldsymbol{E}}$ are the decoupled state, control and disturbance matrices, respectively. In the example given in [34], the decoupled state and control variables include α and β-components for external ac-side current control, α and β-components for internal (balancing) current control and a component for external dc-current control. The ac control variables in $\alpha\beta$-components were in a next step transformed to dq-components using the (time-variant) Park-transform, which resulted in state-space control with similar features as the traditional decoupled dq-control, e.g., described in [25].

The decoupled discrete-time control for MMCs can be designed based on the states defined in (2), possibly augmented with other states to include, e.g., control and sensor delay compensation or states for integral feedback control. The

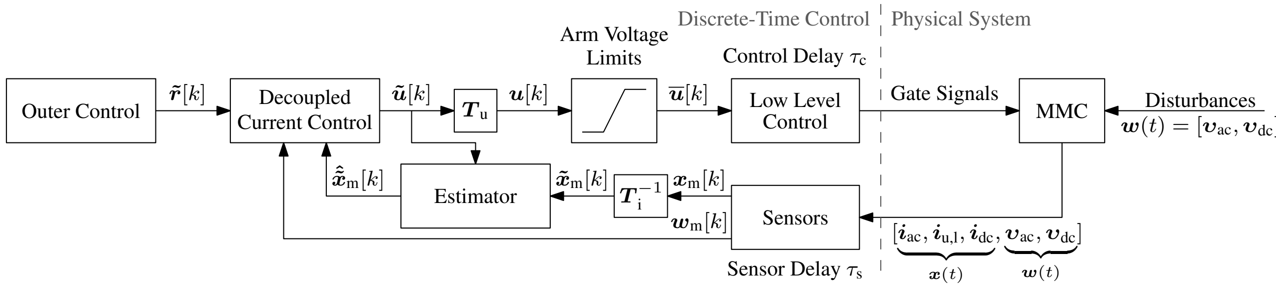


Fig. 2. Diagram of discrete-time MMC current control with state estimator and explicit representation of arm voltage limits and control and sensor delays.

resulting discrete system equation and control law are given by:

$$\begin{aligned}\tilde{\boldsymbol{x}}[k+1] &= \tilde{\boldsymbol{\Phi}}\tilde{\boldsymbol{x}}[k] + \tilde{\boldsymbol{\Gamma}}\tilde{\boldsymbol{u}}[k] + \tilde{\boldsymbol{\mathcal{E}}}\boldsymbol{w}[k] \\ \tilde{\boldsymbol{u}}[k] &= \underbrace{-\tilde{\boldsymbol{K}}\tilde{\boldsymbol{x}}_\mathrm{m}[k]}_{\substack{\text{Proportional}\\ \text{feedback}}} \underbrace{-\tilde{\boldsymbol{\Gamma}}^{-1}\tilde{\boldsymbol{\mathcal{E}}}\boldsymbol{w}_\mathrm{m}[k]}_{\substack{\text{Disturbance}\\ \text{compensation}}} \underbrace{+\tilde{\boldsymbol{N}}\tilde{\boldsymbol{r}}[k]}_{\substack{\text{Reference}\\ \text{tracking}}},\end{aligned} \tag{3}$$

where $\tilde{\boldsymbol{x}}[k]$ and $\tilde{\boldsymbol{u}}[k]$ are the state and control vectors, $\boldsymbol{w}[k]$ and $\tilde{\boldsymbol{r}}[k]$ are the disturbance and input vectors, $\tilde{\boldsymbol{\Phi}}$ and $\tilde{\boldsymbol{\Gamma}}$ are the discretized state and control matrices, and $\tilde{\boldsymbol{\mathcal{E}}}$ is the discretized disturbance matrix. In case an estimator is used, the control acts on the estimated state and disturbance vectors $\hat{\tilde{\boldsymbol{x}}}[k]$ and $\hat{\tilde{\boldsymbol{w}}}[k]$. With an estimator, sensor and control delays can be compensated for by adding states associated with the (delayed) measured state and the control variables, as discussed in detail in [38]. The resulting state variable vector and state, control and proportional gain matrices are denoted by $\tilde{\boldsymbol{x}}'[k]$, $\tilde{\boldsymbol{\Phi}}'$, $\tilde{\boldsymbol{\Gamma}}'$, $\tilde{\boldsymbol{K}}'$, respectively.

The control law in (3) consists of feedforward terms, i.e., those associated with reference tracking and disturbance compensation, and feedback terms, which may consist of proportional feedback and other control terms such as integral feedback and rejection of disturbance inputs other than the ac and dc system voltages. In (3), $\tilde{\boldsymbol{K}}$ and $\tilde{\boldsymbol{N}}$ are the proportional gain matrix and a matrix adapting the reference inputs to reference values for the state variables, respectively. Integral feedback or compensation of harmonic disturbances, as e.g., decribed in [39], have been omitted here for the sake of simplicity. The subscript $_\mathrm{m}$ indicates a measured value, which is delayed by an integer number of samples compared to the actual value.

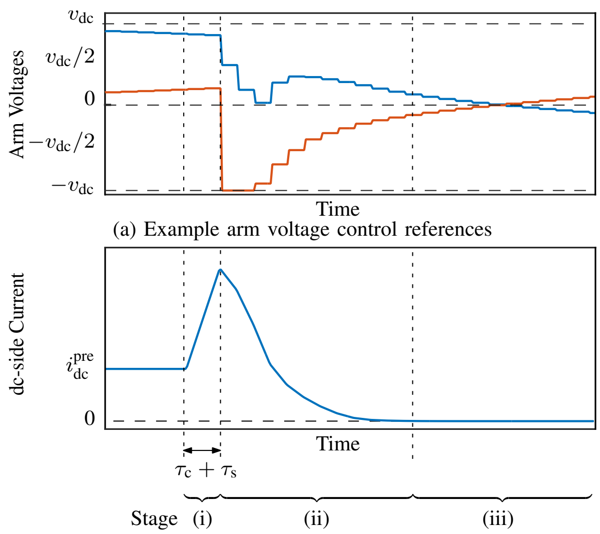
As a final step, the pertinent features of dc-side fault handling are identified, as shown in Fig. 2, by putting the discrete-time current control of the MMC in the context of the outer controls and the physical system of the MMC itself. First, the control actions that counteract disturbances, e.g., those that the dc-side fault causes in the MMC's dc terminal voltage, are delayed by the control and sensor delay. Although the disturbance is directly applied to the MMC, it will only be observed by the current control after a delay caused by the sensors and sampling. The action counteracting the observed disturbance can only be applied to the MMC after a further delay introduced by the controls. The delay on this response to disturbances can, unlike for control inputs, not be compensated for using an estimator [38]. Second, the control actions are restricted by the arm voltage limits, which are imposed by the positive and negative voltage capability of each arm. The negative arm voltage capability depends on the number of submodules in each arm that posesses negative voltage capability and this, in turn, determines the ability of the converter to maintain control during dc-side faults. The negative arm voltage capability that is required to block the infeed of the ac system to the dc-side fault depends on the winding configuration of the converter transformer. This voltage must be at least equal to the amplitude of the ac system's phase voltage v_ac in a star-connected configuration or half the amplitude of the ac systems' line-to-line voltage in a delta-connected configuration, as detailed in [40]. Furthermore, the negative arm voltage capability will determine the dynamic response of the converter during dc-side fault clearing, with more voltage capability resulting in a faster decay of the dc-side fault current.

B. Controlled DC-side Fault Blocking Process

1) DC-Side Current Control: For dc-side pole-to-pole faults, the part of the current control which counteracts the increase of the arm currents is the one associated with the external dc-side current control. The state and control variables of the state equation for the dc-side current control are obtained by (following the derivation in [37]) taking the 0 component of the $\alpha\beta 0$-transform applied to the internal sum currents $i_\Sigma = {}^1\!/_2\,(i_\mathrm{u} + i_\mathrm{l})$ and sum voltages $v_\Sigma = v_\mathrm{u} + v_\mathrm{l}$ of the converter. This yields $i_\Sigma^0 = {}^1\!/_3(i_\Sigma^\mathrm{a} + i_\Sigma^\mathrm{b} + i_\Sigma^\mathrm{c}) = i_\mathrm{dc}$ and $v_\Sigma^0 = {}^1\!/_3(v_\Sigma^\mathrm{a} + v_\Sigma^\mathrm{b} + v_\Sigma^\mathrm{c})$ (see Fig. 1b and Fig. 1c). The resulting state and discrete-time control equation (excluding estimator) are:

$$\begin{aligned}\dot{i}_\mathrm{dc}(t) &= -\frac{1}{L_\mathrm{arm}^\mathrm{eq}}\left(R_\mathrm{arm}^\mathrm{eq} i_\mathrm{dc}(t) - v_\Sigma^0(t) + v_\mathrm{dc}(t)\right), \\ \tilde{u}^\mathrm{dc}[k] &= -\tilde{K}^\mathrm{dc} i_\mathrm{dc,m}[k] + v_\mathrm{dc,m}[k] + \tilde{N}^\mathrm{dc} i^\mathrm{ref,dc}[k],\end{aligned} \tag{4}$$

where, for an MMC in a three-phase application, $L_\mathrm{arm}^\mathrm{eq} = 2/3 L_\mathrm{arm}$ and $R_\mathrm{arm}^\mathrm{eq} = 2/3 R_\mathrm{arm}$. Comparing with (1), it is clear that $A^\mathrm{dc} = -R_\mathrm{arm}^\mathrm{eq}/L_\mathrm{arm}^\mathrm{eq}$, $B^\mathrm{dc} = 1/L_\mathrm{arm}^\mathrm{eq}$ and $E^\mathrm{dc} = -1/L_\mathrm{arm}^\mathrm{eq}$. The control variable $\tilde{u}^\mathrm{dc}[k]$ may consist of a feedback, feedforward and reference term, acting on the measured dc-side current, measured dc-side voltage and reference input current, respectively. The dc component of the arm voltages injected by the MMC $v_\Sigma^0(t)$ is obtained in several steps (cf. Fig. 2). First, the dc component of the decoupled control variable $\tilde{u}^\mathrm{dc}[k]$ is, together with the other decoupled control variables in $\tilde{\boldsymbol{u}}[k]$,



(a) Example arm voltage control references

(b) Dc-side fault current as a function of time

Fig. 3. Three stages in dc-side fault response for converters with controlled fault blocking capability.

transformed to the voltage reference waveform vector $\boldsymbol{u}[k]$ for each of the six arms. Through applying the gate signals corresponding to the saturated value of these arm voltage reference waveforms, $\overline{\boldsymbol{u}}[k]$, the actual inserted arm voltages $v_{\mathrm{u,l}}$ are obtained. The resulting dc component inserted by the MMC, v_{Σ}^{0} is obtained through taking the zero component of the $\alpha\beta 0$-transform of the sum arm voltages.

2) Stages in Controlled DC-side Fault Blocking: During a dc-side fault, the controller will indicate negative arm voltage references, as it attempts to maintain current control. To track these references, the converter arms must be capable of injecting sufficient negative voltage, that is, sufficient to (i) match the ac grid voltage still being applied while the dc-side voltage is at or close to zero and (ii) impose a voltage to maintain control of the arm currents.

The dc-side current of the converter will be instantly affected by the rapid reduction in the dc-side voltage caused by a dc-side fault. With sufficient negative arm voltage available, a well-designed controller may achieve current control on the medium- to long-term with the fault still present, as shown in Fig. 3. However, the current control cannot respond instantaneously to a change in the dc-side voltage disturbance term due to the delays introduced by control and sensors, as noted in Fig. 2. In addition to the sensor and control delays, the available negative voltage capability of the converter restricts the ability of the current control to maintain control at all times during the dc-side fault. During a dc-side fault, the current control sets a large negative voltage reference to counteract the increase in the arm currents. If the reference voltage exceeds the negative voltage capability, the actual voltages inserted by the arms may not match the reference voltage and so the current control may temporarily be lost.

Taking into account the above considerations, the response of a converter to a dc-side fault (assuming the converter has controlled fault blocking capability) occurs in three stages; two transient stages comprising uncontrolled and controlled response and one steady-state stage, as illustrated in Fig. 3. The first stage, stage (i), is characterized by an uncontrolled increase of the fault current and has a length of $\tau_{\mathrm{c}} + \tau_{\mathrm{s}}$ (Fig. 3, stage (i)). In this stage, the arm voltage references remain unchanged compared with the pre-fault conditions as the control actions counteracting the increase in fault current are delayed by the sensor and control delay (Fig. 3a, stage (i)). In the second stage, the current decays as a result of the controls' response (Fig. 3, stage(ii)). The current control must respond sufficiently fast to avoid converter internal quantities to exceed the minimum or maximum values which would otherwise lead to permanent loss of control or damage to components. The response of the current control may depend on its actual implementation, e.g., proportional or proportional-integral. Due to the large increase of the fault current, the arm voltage references may exceed the nominal negative arm voltage limit in this stage (Fig. 3a). In the third stage, the control maintains the dc-side current reference as requested by the converter's protection (Fig. 3, stage (iii)).

III. Fault Current Source Models

In this section, we propose three different forms of converter model, all of which are capable of representing the response of the converter control and protection system to dc-side faults. The first two converter models are suitable for integration in EMT-type (ElectroMagnetic Transient) software and comprise an electrical part in the form of an equivalent circuit and a control and protection part. The third converter model is suitable for transient simulations using frequency domain methods. It represents the converter as a current source of which the response depends on the desired post-fault dc-side current on the one hand and the applied dc-side voltage on the other hand.

A. Preliminary Assumptions

The first assumption concerns which elements of the control system respond fast enough to be relevant to the fault response. For instance, the control which maintains a balance between the extracted ac- and dc-side powers, i.e., which regulates the total energy stored within the MMC, should according to [41] have a bandwidth lower than 10 Hz and is therefore too slow to be relevant to a fault and can be disregarded. The current controller is the only control which is considered within the proposed models since it must have been designed with a response to dc-side faults that is fast enough to maintain the converter currents within safe limits. The controllers on a lower level than the current controller also provide a fast response, but for this study can be disregarded by assuming that the submodules are well-balanced.

Secondly, the converter arms are assumed to be capable of generating any voltage requested by the current controller provided this voltage is within the nominal arm voltage limits. This assumption implies limited variation of the submodule capacitor voltages during the first two stages of the dc-side fault clearing process. As a consequence of this assumption, the proposed models do not represent individual submodules nor variations in the available arm voltages and assume no significant control effort is needed for the internal energy balancing controls. The proposed models thus assume a voltage source with fixed minimum and maximum values that represent the nominal minimum and maximum voltage capabilities of the arms.

Thirdly, it is assumed that upon detection of a dc-side fault, the protection system will set the reference values for the dc-side current and the active power component of the ac-side current to zero. The actual implementation of the protection system is not a major subject of investigation in this paper. The protection system must detect dc-side faults and may set the dc-side current reference to a desired value. The detection of dc-side faults may be done using measurements in the dc system (e.g., in the dc lines, at the dc bus) or in the converter itself [42]. The dc-side current reference as set by the protection may be set to any of the possible values within the operational limits of the converter, as the converter is assumed to have sufficient negative voltage capability to maintain current control in the mid-fault steady-state. Although any reference can be set, for the studies in this paper, a value of zero is adopted for the sake of simplicity.

B. Models for EMT-type software

Two models for use in EMT-type software are proposed. These are further referred to as the "three-phase EMT-type"- and "dc EMT-type"-model. The three-phase EMT-type model might be preferred when accurate data of the ac system and all current control loops are available, e.g., in system studies with detailed converter specifications. The dc EMT-type model ignores all ac-side dynamics and might be preferred when less specific data is available and when the basic shape of the waveforms is of interest rather than precise values, such as in preliminary system studies.

1) Equivalent Circuit: The equivalent circuit of the three-phase EMT-type model consists of a representation of the three converter legs and the dc and ac interfaces (Fig. 1a). The voltage sources in the equivalent circuit insert arm voltages according to the delayed and saturated references generated by the discrete-time control (with conversion to the continuous time domain using a zero-order hold):

$$\boldsymbol{u}(t) = \sum_{k=-\infty}^{k=\infty} \overline{\boldsymbol{u}}[k] \mathrm{rect}\left(\frac{t-\tau_c-T_\mathrm{s}/2-kT_\mathrm{s}}{T_\mathrm{s}}\right), \tag{5}$$

in which "rect" represents the rectangular function and T_s is the sampling interval of the discrete-time controller.

The equivalent circuit of the dc EMT-type model consists of a controllable voltage source in series with $L_\mathrm{arm}^\mathrm{eq}$ and $R_\mathrm{arm}^\mathrm{eq}$ (cf. Fig. 1c). In the equivalent circuit model, the voltage source injects $\upsilon_\Sigma^{0\,\prime}(t)$, which is determined using the converter control and the sum of the positive and negative arm voltage limits, $\upsilon_\Sigma^{0,\mathrm{max}}$ and $\upsilon_\Sigma^{0,\mathrm{min}}$:

$$\begin{aligned} \tilde{u}_\mathrm{d}^\mathrm{dc}(t) &= \sum_{k=-\infty}^{k=\infty} \tilde{u}^\mathrm{dc}[k] \mathrm{rect}\left(\frac{t-\tau_c-T_\mathrm{s}/2-kT_\mathrm{s}}{T_\mathrm{s}}\right) \\ \upsilon_\Sigma^{0\,\prime}(t) &= \begin{cases} \upsilon_\Sigma^{0,\mathrm{min}} & \text{if } \tilde{u}_\mathrm{d}^\mathrm{dc}(t) \leq \upsilon_\Sigma^{0,\mathrm{min}} \\ \tilde{u}_\mathrm{d}^\mathrm{dc}(t) & \text{if } \upsilon_\Sigma^{0,\mathrm{min}} < \tilde{u}_\mathrm{d}^\mathrm{dc}(t) < \upsilon_\Sigma^{0,\mathrm{max}} \\ \upsilon_\Sigma^{0,\mathrm{max}} & \text{if } \upsilon_\Sigma^{0,\mathrm{max}} \leq \tilde{u}_\mathrm{d}^\mathrm{dc}(t) \end{cases} . \end{aligned} \tag{6}$$

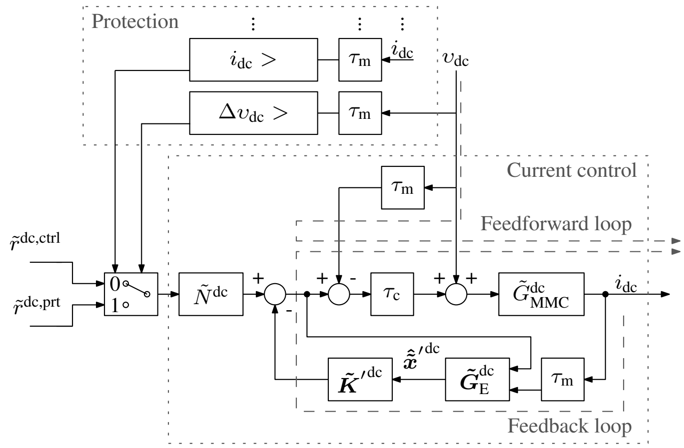


Fig. 4. Block diagram of converter dc-side current control and protection considering the dc-side voltage as disturbance.

The fact that $\upsilon_\Sigma^{0\,\prime}(t)$ is not equal to $\upsilon_\Sigma^{0}(t)$ in (4) entails important consequences for the accuracy of this model. The dc equivalent model has been found to be as accurate as the three-phase EMT-type model only if arm voltage limits are not hit, as only in that case $\upsilon_\Sigma^{0\,\prime}(t) = \upsilon_\Sigma^{0}(t)$. In case the arm voltage limits are hit, $\upsilon_\Sigma^{0\,\prime}(t) \neq \upsilon_\Sigma^{0}(t)$ as the arm voltage limits apply differently to the requested voltage waveforms. In (4), the value of $\upsilon_\Sigma^{0}(t)$ is obtained after applying the arm voltage limits to $\boldsymbol{u}(t)$, which takes into account the combined action of the controls associated with all control variables. In (6), the sum arm voltage limits are applied only to $\tilde{u}_\mathrm{d}^\mathrm{dc}(t)$, i.e., in the absence of the other control variables.

2) Control and Protection: For the three-phase EMT-type model, the converter current control (shown in Fig. 2) must be represented in its entirety whereas the outer controls are omitted. This current control may be designed using (3), in which the state variable is a vector of independent currents and the control variable is a vector of voltages, as discussed in Section II. Besides the dc-side current control, the inclusion of current control associated with ac and converter internal currents provides the user with the possibility to represent pre-fault conditions and to accurately implement arm voltage limits. In case the current control itself is not decoupled, the decoupled current references must be transformed to the quantities associated with the current control's state variables, e.g., the converter arm currents.

The dc EMT-type model requires modeling of the dc-side current control (cf. (4) in Section II and Fig. 4), possibly complemented with a saturation limit to represent the negative voltage capability. The dc-side current control is readily available in case of decoupled current control. If the current control is not decoupled, the dc-side current control must be extracted using decoupling transformations, e.g., based on the $\alpha\beta0$-transform. The dc-side current control allows the user to set a pre-fault dc-side current. As shown in (6), positive and negative sum arm voltage limits can be implemented thereby taking into account that these are applied only to the control request associated with the dc-side current control.

C. Transfer Function Model

To represent the converter within a frequency domain method for EMT-studies, a model is proposed which represents the converter as a current source responding to the disturbance caused by the dc-side voltage. A linear model without any limits allows for a frequency domain method without implementation of any switch events (in the absence of other elements introducing discontinuities). In this paper, a discrete-time transfer function model is derived, which is in the paper further referred to as "transfer function model".

The transfer function model is based on a generic plant model of the MMC, its current control and protection (Fig. 4). The dc part of the MMC transfer function, $\tilde{G}^{\mathrm{dc}}_{\mathrm{MMC}}$, is obtained using the dc components of the transformed discrete state and control matrices $\tilde{\boldsymbol{\Phi}}$ and $\tilde{\boldsymbol{\Gamma}}$. In Fig. 4, the dc-side current control is for the sake of simplicity represented as a state feedback proportional control with an estimator, although it might also take other forms such as state feedback control with integral action or disturbance rejection. In normal operation, it takes a reference current as input $\tilde{r}^{\mathrm{dc,ctrl}}$ and in case of faults takes a current reference as set by the protection, $\tilde{r}^{\mathrm{dc,prt}}$. The part of the proportional gain matrix $\tilde{\boldsymbol{K}}'$ associated with the dc-side current control, $\tilde{\boldsymbol{K}}'^{\mathrm{dc}}$ acts on the part of the estimated state vector associated with the dc-side current control $\hat{\tilde{\boldsymbol{x}}}'^{\mathrm{dc}}$, which contains the estimated dc-side current and may also contain state variables to compensate sensor and control delays. The fact that the converter can only control the current after the sensor and control delay is again explicitly present in the block diagram. As shown in Fig. 4, the sensor and control delays are present in the feed-forward and feedback loop.

Based on this framework and the assumption of a fixed delay between the protection action and the instant of fault inception, a transfer function can be constructed which can be used to calculate the dc-side current $i_{\mathrm{dc}}[k]$ as a function $\tilde{r}^{\mathrm{dc,prt}}[k]$ and $\upsilon_{\mathrm{dc}}[k]$. The dc-side current $i_{\mathrm{dc}}[k]$ is calculated as the inverse z-transform of $I_{\mathrm{dc}}(z)$:

$$\begin{aligned}I_{\mathrm{dc}}(z) = &\frac{\tilde{N}^{\mathrm{dc}}\tilde{G}^{\mathrm{dc}}_{\mathrm{MMC}}\xi_1 z^{-k_{\mathrm{s}}}z^{-k_{\mathrm{c}}}}{1+\tilde{G}^{\mathrm{dc}}_{\mathrm{MMC}}\xi_1\xi_2 z^{-k_{\mathrm{s}}}z^{-k_{\mathrm{c}}}}\tilde{R}^{\mathrm{dc,prt}}(z)\\ &+\frac{\tilde{G}^{\mathrm{dc}}_{\mathrm{MMC}}\left(1-z^{-k_{\mathrm{s}}}z^{-k_{\mathrm{c}}}\right)}{1+\tilde{G}^{\mathrm{dc}}_{\mathrm{MMC}}\xi_1\xi_2 z^{-k_{\mathrm{s}}}z^{-k_{\mathrm{c}}}}\mathcal{U}_{\mathrm{dc}}(z),\end{aligned} \tag{7}$$

in which $\tilde{R}^{\mathrm{dc,prt}}(z)$ and $\mathcal{U}_{\mathrm{dc}}(z)$ are the z-transforms of $\tilde{r}^{\mathrm{dc,prt}}[k]$ and $\upsilon_{\mathrm{dc}}[k]$, respectively. Furthermore, $k_{\mathrm{c}} = \lfloor \tau_{\mathrm{c}}/T_{\mathrm{s}} \rceil$, $k_{\mathrm{s}} = \tau_{\mathrm{s}}/T_{\mathrm{s}}$, $\xi_1 = (1+\tilde{\boldsymbol{K}}'^{\mathrm{dc}}\boldsymbol{\chi_1})^{-1}$, and $\xi_2 = \tilde{\boldsymbol{K}}'^{\mathrm{dc}}\boldsymbol{\chi_2}$. $\boldsymbol{\chi_1}$ and $\boldsymbol{\chi_2}$ are the transfer functions associated with the estimator $\tilde{\boldsymbol{G}}^{\mathrm{dc}}_{\mathrm{E}}$, describing the relationship between the estimator's output $\hat{\tilde{\boldsymbol{x}}}'^{\mathrm{dc}}[k]$ with the dc component of the converter's input reference voltage, $\tilde{u}^{\mathrm{dc}}[k]$ and the measured dc-side current $i_{\mathrm{dc,m}}[k]$:

$$\boldsymbol{\chi_1} = \boldsymbol{\chi_3}\left(z^{-1}\left(\boldsymbol{I}-\tilde{\boldsymbol{L}}'^{\mathrm{dc}}\tilde{\boldsymbol{H}}'^{\mathrm{dc}}\right)\tilde{\boldsymbol{\Gamma}}'^{\mathrm{dc}}\right) \tag{8}$$

$$\boldsymbol{\chi_2} = \boldsymbol{\chi_3}\tilde{\boldsymbol{L}}'^{\mathrm{dc}}, \text{where} \tag{9}$$

$$\boldsymbol{\chi_3} = \left(\boldsymbol{I}+z^{-1}\left(\tilde{\boldsymbol{L}}'^{\mathrm{dc}}\tilde{\boldsymbol{H}}'^{\mathrm{dc}}-\boldsymbol{I}\right)\tilde{\boldsymbol{\Phi}}'^{\mathrm{dc}}\right)^{-1}. \tag{10}$$

TABLE II
PARAMETERS OF SIMULATION MODEL AND LAB-SCALE CONVERTER PROTOTYPE

Parameter	Value
Rated dc power	15 kW
dc pole-to-pole voltage	1500 V
ac line voltage	780.77 V
Transformer leakage inductance	0.15 pu
Arm inductance L_{arm}	0.17 pu
Arm resistance (estimated) R_{arm}	0.04 pu
Number of submodules per arm	10
Nominal converter energy storage	49.5 kJ/MVA
Submodule type	Half/Full-bridge
Ratio half-/full-bridge submodules	0 or 0.5

where $\tilde{\boldsymbol{\Phi}}'^{\mathrm{dc}}$, $\tilde{\boldsymbol{\Gamma}}'^{\mathrm{dc}}$, $\tilde{\boldsymbol{H}}'^{\mathrm{dc}}$ and $\tilde{\boldsymbol{L}}'^{\mathrm{dc}}$ are the parts of the discrete-time state, control, output and estimator gain matrices associated with the dc-side current control, respectively, and $\boldsymbol{I}$ is the identity matrix. The output matrix $\tilde{\boldsymbol{H}}'^{\mathrm{dc}}$ selects the state variables associated with the dc-side current.

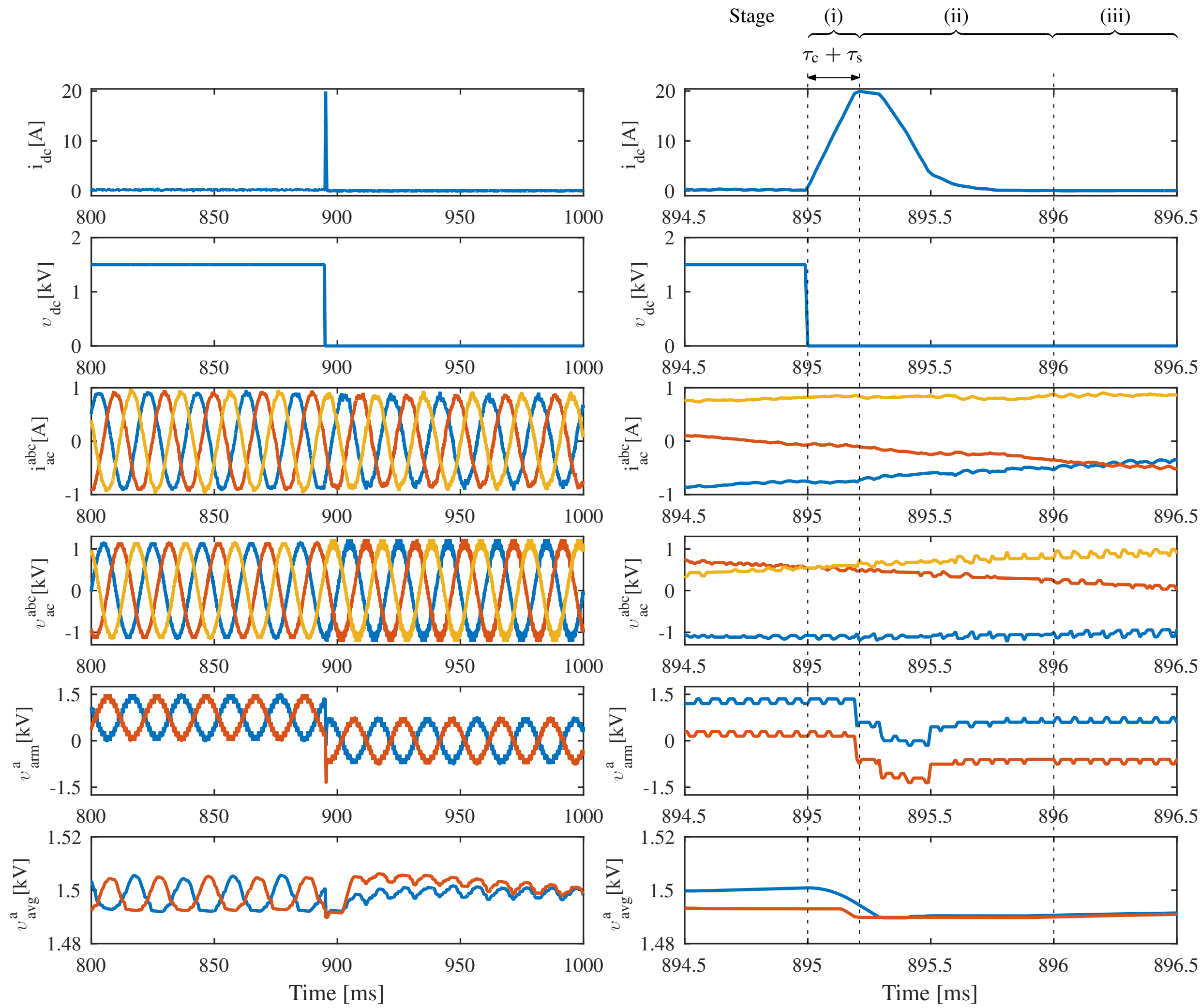
IV. Model Validation

In this section, the proposed models are validated by comparing their output waveforms against those of a detailed (full-switching) simulation model and against results obtained from experiments with a lab-scale hardware converter. The lab-scale converter prototype is described in [43], [44]. The most important model parameters, control and protection are described below.

A. Model Parameters and Control

1) Simulation Model and Parameters: The detailed simulation model, based on the experimental converter described in [44], incorporates outer controls such as active and reactive power control, horizontal and vertical energy balancing control and inner controls such as current and submodule voltage control. All controls were taken from [44], except for the current control which is based on the control proposed in [34]. The model parameters are based on the lab-scale converter prototype described in [44]. These parameters are recapitulated in Table II. The converter topology may be full-bridge or hybrid with 50 % full- and 50 % half-bridge submodules. Unless stated otherwise, the current control is designed using $\rho = 0.5$ and a control and sensor delay of 100 μs each is assumed.

2) Current Control: The implemented current control is a state feedback proportional control where the state vector is augmented for control and sensor delay compensation. The non-augmented state, input and disturbance vectors $\boldsymbol{x}$, $\boldsymbol{u}$ and $\boldsymbol{w}$ are $[i^{\mathrm{a}}_{\mathrm{ac}}, i^{\mathrm{b}}_{\mathrm{ac}}, i^{\mathrm{c}}_{\mathrm{u}}, i^{\mathrm{a}}_{\mathrm{l}}, i_{\mathrm{dc}}]^T$, $[\upsilon^{\mathrm{a}}_{\mathrm{u}}, \upsilon^{\mathrm{a}}_{\mathrm{l}}, \upsilon^{\mathrm{b}}_{\mathrm{u}}, \upsilon^{\mathrm{b}}_{\mathrm{l}}, \upsilon^{\mathrm{c}}_{\mathrm{u}}, \upsilon^{\mathrm{c}}_{\mathrm{l}}]^T$ and $[\upsilon^{\mathrm{a}}_{\mathrm{ac}}, \upsilon^{\mathrm{b}}_{\mathrm{ac}}, \upsilon^{\mathrm{c}}_{\mathrm{ac}}, \upsilon_{\mathrm{dc}}]^T$, respectively (see Fig. 1a). To simplify the analysis, as in [34], the state vector is transformed to $\tilde{\boldsymbol{x}} = [i^{\alpha}_{\mathrm{ac}}, i^{\beta}_{\mathrm{ac}}, i^{\alpha}_{\Sigma}, i^{\beta}_{\Sigma}, i_{\mathrm{dc}}]^T$, where $i^{\alpha}_{\mathrm{ac}}, i^{\beta}_{\mathrm{ac}}$ and $i^{\alpha}_{\Sigma}, i^{\beta}_{\Sigma}$ are the ac external and converter internal currents in the $\alpha\beta 0$-reference frame, respectively. It should be noted that an ac-side zero component has been omitted here and that the dc-side current is the zero component of the converter internal currents. The control input



(a) (b)

Fig. 5. Fault response of a full-bridge MMC showing dc-side current, dc-side voltage, ac-side current, ac-side voltages, upper arm (blue) and lower arm (red) voltage of phase A and the average sum submodule voltage for upper (blue) and lower arm (red) of phase A. A dc-side fault was applied at t=895 ms. Subplots (a) show signals over 200 ms and subplots (b) show detail over 2 ms around fault inception.

vector is transformed to $\tilde{\boldsymbol{u}} = [v_u^\alpha, v_u^\beta, v_l^\alpha, v_l^\beta, v_{dc}]^T$, where v_u^α, v_u^β and v_l^α, v_l^β are the upper and lower arm voltages in the $\alpha\beta 0$-reference frame, respectively. The transformation matrices $\boldsymbol{T}_i$ and $\boldsymbol{T}_u$ are (based on the approach followed in [34]):

$$\boldsymbol{T}_i = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ -1/2 & \sqrt{3}/2 & 0 & 0 & 0 \\ -1/4 & -\sqrt{3}/4 & -1/2 & -\sqrt{3}/2 & 1/3 \\ -1/2 & 0 & 1 & 0 & 1/3 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix}, \tag{11}$$

$$\boldsymbol{T}_u = \begin{bmatrix} 1 & 0 & 0 & 0 & 1/2 \\ -1/2 & \sqrt{3}/2 & 0 & 0 & 1/2 \\ -1/2 & -\sqrt{3}/2 & 0 & 0 & 1/2 \\ 0 & 0 & 1 & 0 & 1/2 \\ 0 & 0 & -1/2 & \sqrt{3}/2 & 1/2 \\ 0 & 0 & -1/2 & -\sqrt{3}/2 & 1/2 \end{bmatrix}. \tag{12}$$

The resulting transformed state and control matrices $\tilde{\boldsymbol{\Phi}}$ and $\tilde{\boldsymbol{\Gamma}}$ are derived from the transformed continuous state-space matrices:

$$\tilde{\boldsymbol{A}} = -\,\mathrm{diag}\left\{R'_{ac}/L'_{ac},\, R'_{ac}/L'_{ac},\, R_{arm}/L_{arm},\, R_{arm}/L_{arm},\, R_{arm}/L_{arm}{}^{*}\right\}, \tag{13}$$

$$\tilde{\boldsymbol{B}} = \begin{bmatrix} 1/2L'_{ac} & 0 & -1/2L'_{ac} & 0 & 0 \\ 0 & 1/2L'_{ac} & 0 & -1/2L'_{ac} & 0 \\ 1/2L_{arm} & 0 & 1/2L_{arm} & 0 & 0 \\ 0 & 1/2L_{arm} & 0 & 1/2L_{arm} & 0 \\ 0 & 0 & 0 & 0 & 1/L_{arm}^{eq}{}^{\dagger} \end{bmatrix}, \tag{14}$$

in which $R'_{ac} = R_{arm}/2 + R_{ac}$ and $L'_{ac} = L_{arm}/2 + L_{ac}$. To take into account control and sensor delays, the state and input vectors and dynamics and control matrices are augmented to $\tilde{\boldsymbol{x}}', \tilde{\boldsymbol{u}}', \tilde{\boldsymbol{\Phi}}', \tilde{\boldsymbol{\Gamma}}'$, according the methods described in [38]. Although in (14), further decoupling of the control matrix is possible in ac-side quantities, for the purpose of our studies, the decoupling of the ac- and dc-side control is sufficient.

*If a dc-side inductance and resistance R_{dc} and L_{dc} are present, this entry becomes $(R_{arm}^{eq}+R_{dc})/(L_{arm}^{eq}+L_{dc})$ (e.g., see also [45].)

†If a dc-side inductance L_{dc} is present, this entry becomes $1/(L_{arm}^{eq}+L_{dc})$.

Using these matrices, the current control is implemented as a state feedback proportional control with estimator and reference input tracking (similar to Fig. 4). The proportional feedback control gain matrix $\boldsymbol{K}$ is designed as a linear quadratic regulator using the base cost matrices $\boldsymbol{Q}$ and $\boldsymbol{R}$ which are defined as (taking a similar approach as outlined in [38]):

$$\begin{aligned}\boldsymbol{Q} &= \operatorname{diag}\left\{{}^{1}/{I_{\mathrm{ac}}^2}, {}^{1}/{I_{\mathrm{ac}}^2}, {}^{1}/{I_{\mathrm{arm}}^2}, {}^{1}/{I_{\mathrm{arm}}^2}, {}^{1}/{I_{\mathrm{dc}}^2}\right\} \\ \boldsymbol{R} &= \rho \operatorname{diag}\left\{{}^{1}/{U_{\mathrm{dc}}^2}, {}^{1}/{U_{\mathrm{dc}}^2}, {}^{1}/{U_{\mathrm{dc}}^2}, {}^{1}/{U_{\mathrm{dc}}^2}, {}^{1}/{U_{\mathrm{dc}}^2}\right\},\end{aligned} \tag{15}$$

where I_{ac}, I_{arm}, I_{dc} and U_{dc} are the currents and dc voltage associated with the nominal powers and voltages of Table II.

To design the gain matrix $\tilde{\boldsymbol{K}}'$ for the augmented and transformed control variables, $\boldsymbol{Q}$ and $\boldsymbol{R}$ are augmented to diagonal matrices $\boldsymbol{Q'}$ and $\boldsymbol{R'}$, considering zero entries for the augmented state vector variables associated with sensor delay compensation and replicas of $\boldsymbol{R}$ for the augmented state and control variables associated with the control delay compensation. The matrix $\tilde{\boldsymbol{N}}'$ transforms the reference inputs to the appropriate reference state variables and is determined according to the method described in [38].

The method shown above is only one method to tune the converter parameters, whereas other methods or rules of thumb have equally been used in the literature (e.g., see [24]). For this paper, the method above is considered sufficient to assess the impact of the current control gain, given control and sensor delays, by varying the design parameter ρ.

3) Protection: The protection sets the reference values of the active component of the ac- and dc-side current to zero when it detects a dc-side fault. A dc-side fault is detected when the dc pole-to-pole voltage falls below 30 % of its nominal value or whenever the absolute difference between the positive and negative dc pole-to-ground voltage exceeds 40% of the pole-to-pole voltage. For demonstration purposes, the dc-side current reference in each arm is set to zero via a zero active power reference. As the protection does not alter the reactive power reference, the converter retains the ability to operate as a STATCOM during dc-side faults.

B. Simulation Verification - Full-Bridge MMC

1) Detailed Analysis of Fault Current Control of Full-Bridge MMC: A detailed analysis of an example of the dc-side fault current control of the full-bridge MMC allows us to verify the analysis of Section II and the assumptions made in Section III-A. The example used for the analysis is a solid short circuit at the dc terminals of the full-bridge MMC under zero-load conditions. The results for the example were obtained with the detailed simulation model as described in the previous section.

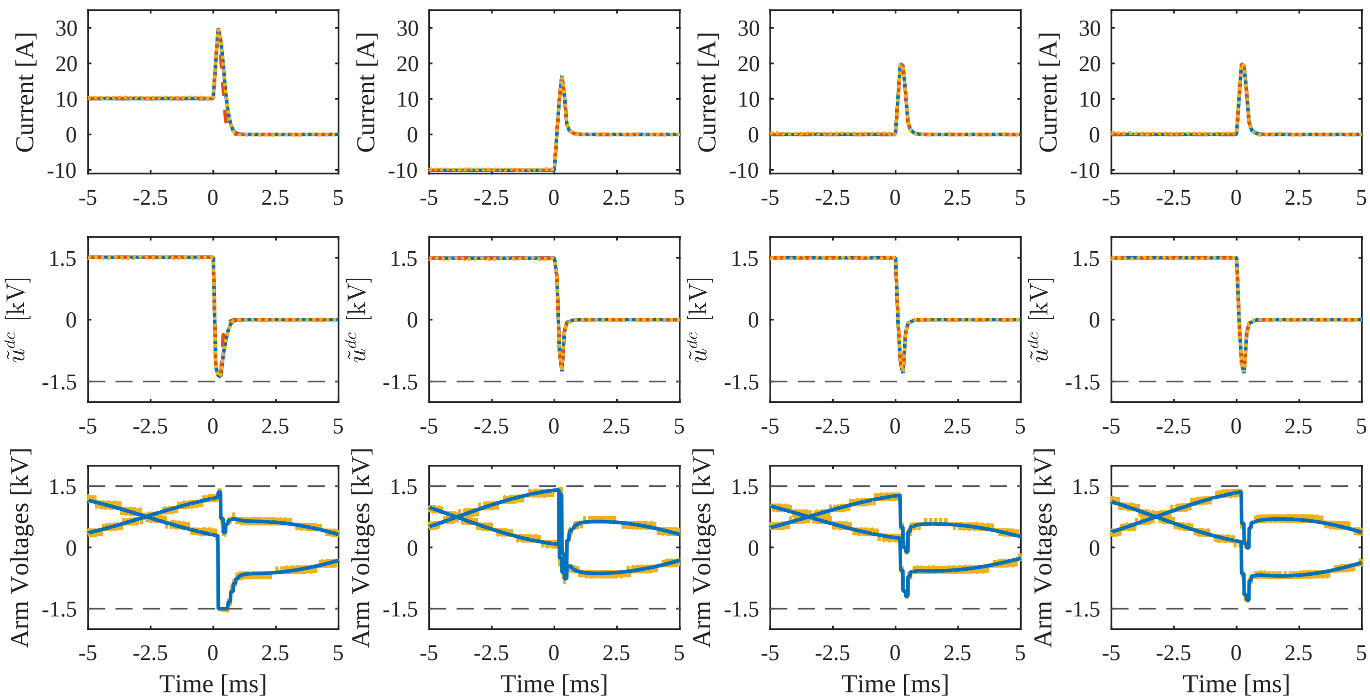
The three stages of the dc-side fault current handling can be observed in the dc-side current and phase A arm voltages (top and fifth plots of Fig. 5). The first stage can be observed in the increase of the dc-side current, which increases up to a value of 20 A. This stage lasts for 200 μs, which is the sum of the control and sensor delays. During this stage, the control system has not responded to the fault and arm voltages are seen to continue the same pattern. As a consequence, the current rise is not arrested. The second stage starts when the arm voltages begin to respond to the dc-side fault and can be observed in the abrupt decrease of the phase A arm voltages. There follows a reduction of the dc-side current to zero. In the third stage, after the dc-side current has reached zero, the phase A arm voltages alternate around zero instead of around half the dc-side voltage.

The assumption that energy balancing is retained during a dc-side fault, i.e., the second assumption in Section III-A, is verified by the observation that minimum and maximum submodule voltages do not diverge significantly and remain within acceptable limits (sixth plot in Fig. 5). Although not shown, the energy balancing control only requires a small control effort to maintain this balance. As a result, the voltage requested by the energy balancing control does not considerably influence the total requested arm voltage and is therefore omitted in the proposed models.

2) Comparison of detailed model with EMT-type models: To verify the accuracy of the waveforms generated during a fault by the proposed models for EMT-type simulations, waveforms from each are compared against the waveforms generated by the detailed simulation model. The comparison involves four cases with following pre-fault power flow: Case (I) 1.0 pu rectifying active power, Case (II) 1.0 pu inverting active power, Case (III) 0.5 pu inductive reactive power and Case (IV) 0.5 pu capacitive reactive power. The accuracy of the proposed models is analyzed using following quantities: the dc-side current, the requested dc-side voltage, $\tilde{u}^{\mathrm{dc}}[k]$ and the phase A arm voltages $v_{\mathrm{u}}^{\mathrm{a}}$ and $v_{\mathrm{l}}^{\mathrm{a}}$. The simulations for the full-bridge case are shown in Fig. 6 and, to facilitate comparison, the simulations for the hybrid case described in Section IV-C are shown in Fig. 7.

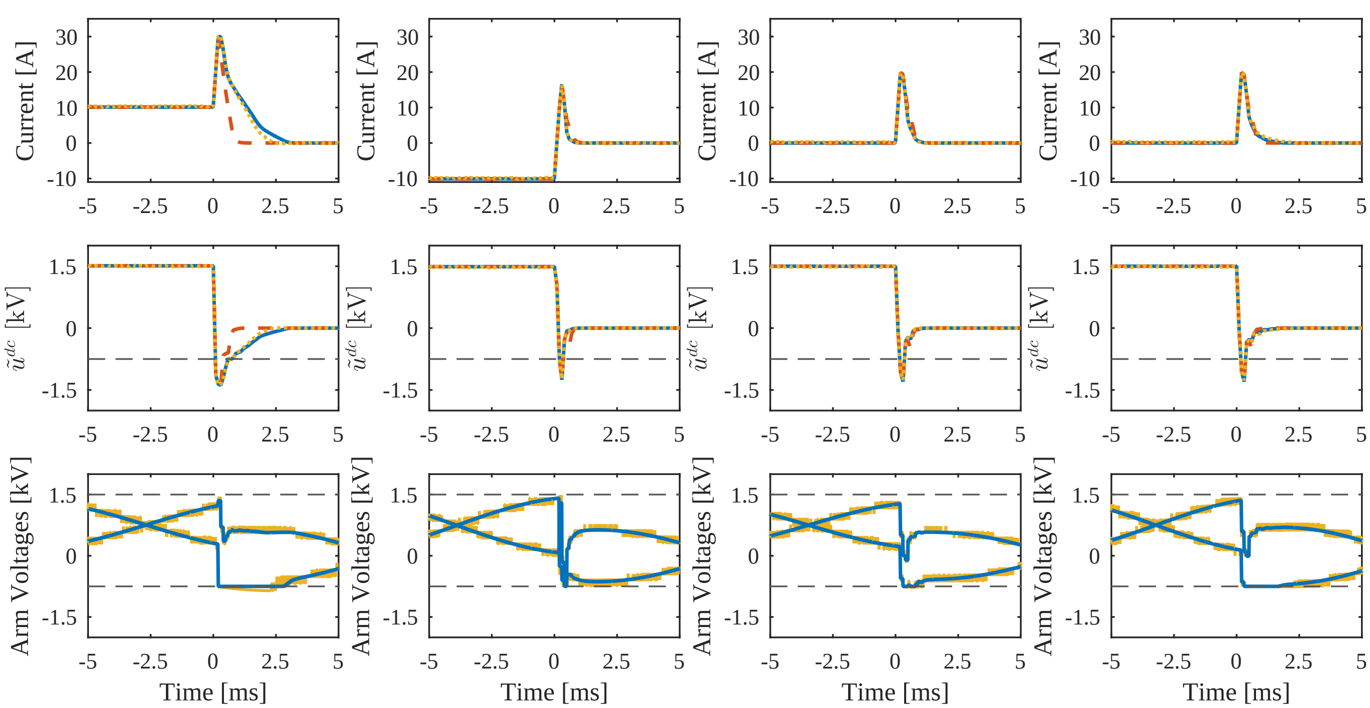
In all cases, the close match between the dc-side current of the three-phase EMT-type and the detailed model (seen in Fig. 6) supports the assumption that, under balanced initial conditions, control loops other than the current control may be excluded without significant loss of accuracy. It can be seen that the inner (submodule voltage balancing) control loops do not greatly affect the dc-side current in that the proposed three-phase EMT-type model produces the same dc-side current as the detailed model (Fig. 6). Second, the outer (energy balancing) control loops do not greatly affect the dc-side current, as, under the same initial conditions, the requested arm voltage by the three-phase EMT-type and detailed model is almost the same.

The case of 1.0 pu rectifying power (Case (I)) provides evidence which supports the second assumption of Section III-A. In this case, the converter arms are capable of inserting a voltage close to -1.5 kV, i.e., the nominal negative arm voltage limit. This demonstrates that the sum arm voltage did not decrease significantly during stage (i) of the dc-side fault clearing process. However, there is a slight mismatch between the three-phase EMT-type model and the detailed model. This mismatch stems from the fact that all submodule capacitors charge when simultaneously inserted for a certain amount of time, as is the case when a nominal arm voltage limit is hit. The decaying arm current charges all submodule capacitors and hence increases the negative arm voltage beyond the



(a) P = 1.0 pu, Q = 0 pu (b) P = -1.0 pu, Q = 0 pu (c) P = 0 pu, Q = 0.5 pu (d) P = 0 pu, Q = -0.5 pu

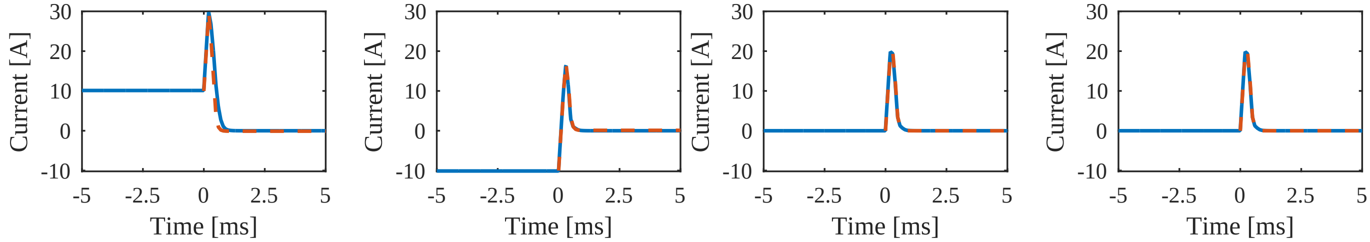
Fig. 6. Full-bridge case - Comparison of i_{dc}, $u_{\mathrm{dc}}^{\mathrm{ctrl}}$ and arm voltage output of three-phase EMT-type (solid blue line), dc EMT-type (dashed red line) and detailed model (yellow dotted line).



(a) P = 1.0 pu, Q = 0 pu (b) P = -1.0 pu, Q = 0 pu (c) P = 0 pu, Q = 0.5 pu (d) P = 0 pu, Q = -0.5 pu

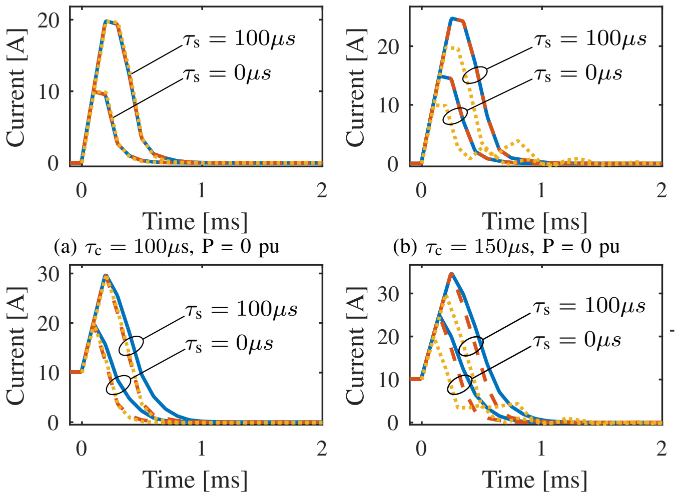
Fig. 7. Hybrid case - Comparison of i_{dc}, $u_{\mathrm{dc}}^{\mathrm{ctrl}}$ and arm voltage output of three-phase (solid blue line), dc EMT-type (dashed red line) and detailed model (yellow dotted line).

nominal negative arm voltage limit. Given that the three-phase EMT model uses a constant negative arm voltage limit, it underestimates the actually inserted voltage. Furthermore, there is a mismatch between the three-phase and dc EMT-type model. This mismatch stems from the fact that the dc EMT-type model does not accurately take into account the arm



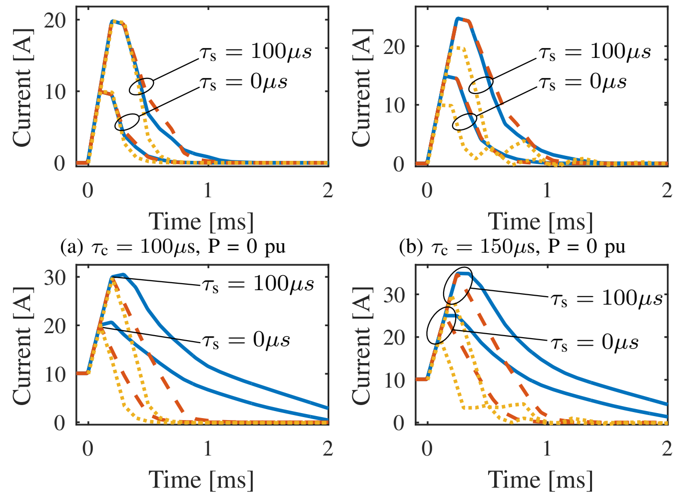
(a) P = 1.0 pu, Q = 0 pu (b) P = -1.0 pu, Q = 0 pu (c) P = 0 pu, Q = 0.5 pu (d) P = 0 pu, Q = -0.5 pu

Fig. 8. Comparison of i_{dc} of three-phase EMT-type (solid blue line) and transfer function model (dashed red line).



(a) $\tau_{\mathrm{c}} = 100\mu s$, P = 0 pu (b) $\tau_{\mathrm{c}} = 150\mu s$, P = 0 pu (c) $\tau_{\mathrm{c}} = 100\mu s$, P = 1 pu (d) $\tau_{\mathrm{c}} = 150\mu s$, P = 1 pu

Fig. 9. Full-bridge case - Comparison of i_{dc} of three phase EMT-type (solid blue line), dc EMT-type (dashed red line) and transfer function model (dotted yellow line) for 100 and 150 μs additional control delay. Sensor delays vary from 0 to 100 μs.



(a) $\tau_{\mathrm{c}} = 100\mu s$, P = 0 pu (b) $\tau_{\mathrm{c}} = 150\mu s$, P = 0 pu (c) $\tau_{\mathrm{c}} = 100\mu s$, P = 1 pu (d) $\tau_{\mathrm{c}} = 150\mu s$, P = 1 pu

Fig. 10. Hybrid case - Comparison of i_{dc} of three phase EMT-type (solid blue line), dc EMT-type (dashed red line) and transfer function model (dotted yellow line) for 100 and 150 μs additional control delay. Sensor delays vary from 0 to 100 μs.

voltage limits because the ac-side dynamics are neglected. In conclusion, Case (I) emphasizes the importance of including the available negative voltage capability in modeling the response of a fault blocking converter to dc-side faults. This limit becomes more important as the negative voltage capability decreases or gain K_{dc} increases because the mismatch between requested and available arm voltage increases under both conditions.

It is important to note that, within the current control, the controlled variables at the ac and dc sides become coupled when the nominal arm voltage limits are reached. For instance, in the case of rectifying active power, the current control must reduce the active power at the ac and dc side to zero (or to the desired post-fault value) simultaneously and it does so by providing components for the arm voltage reference for control of both ac and dc-side quantities. If the nominal arm voltage limits are reached, the available arm voltage must be distributed between the requests for ac and dc-side control contribution, and thereby the two quantities are coupled. This phenomenon was not observed in the cases of inverting active power and pure reactive power modes (Cases (II)-(IV)), because in the former case the requested arm voltages did not reach any limits and in the latter case, no control action is required concerning ac-side quantities (as long as the protection system does not change the pre-fault reactive power reference). In conclusion, for circumstances in which nominal arm voltage limits are reached, the three-phase EMT-type model provides more accurate results than the dc EMT-type model because the three-phase EMT-type model can incorporate the ac system characteristics and therefore those ac quantities in the arm voltages which influence the dc-side fault response.

3) Comparison of three phase EMT-type with transfer function model: To verify the accuracy of the dc-side fault current produced by the transfer function model given in (7), it is compared with the three-phase EMT-type model. The comparison considers the same cases (Case (I)-(IV)) as defined in the previous section.

As for the dc EMT-type model, the waveforms for the transfer function model and the three-phase EMT-type model match except for Case (I) (Fig. 8). This demonstrates that the transfer function model has not lost any pertinent information (compared with the three-phase EMT-type model) except in conditions where a nominal arm voltage limit is reached. It is noteworthy that, in case of active power transfer, the transfer function model is able to take into account pre-fault power flow through the term in (7) associated with $\tilde{r}^{\mathrm{dc,prt}}$.

4) Assessment of influential parameters on model accuracy: The relative performance of the dc EMT-type model and the transfer function model are investigated for changes in control and sensor delays, and current control proportional gain.

For zero power transfer, the dc-side current waveforms for

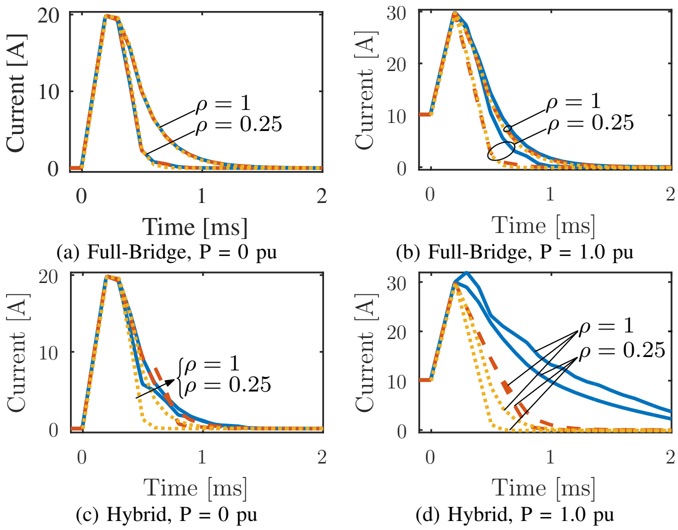


Fig. 11. Comparison of i_{dc} of three phase EMT-type (solid blue line), dc EMT-type (dashed red line) and transfer function model (dotted yellow line) for varying current control gain.

the three-phase and dc EMT-type model match for all control and sensor delays, whereas those of the transfer function only match to the EMT-type models if the control delay is an integer multiple of the control time step (Fig. 9). The latter observation is due to the execution of the transfer function model at the control time step, which is necessary to impose discrete-time control. The accuracy of the transfer function model increases as the control delay draws nearer to a multiple of the control time step. The observations are similar for the case with zero load conditions and that with 1.0 pu rectifying active power, although in the latter case, the arm voltage limits come into play. The dc EMT-type and transfer function model are no longer able to reproduce the result of the three-phase EMT-type model. The waveforms of the former two models do match, but only if the delay is an integer multiple of control time step.

A change in the current control gain has no impact on the accuracy of the dc EMT-type and transfer function model except for the case in which the nominal arm voltage limits are hit (Fig. 11). In case the nominal arm voltage limits are hit, a lower current control gain results in a better match between the waveforms of the dc EMT-type and transfer function model compared to those of the three-phase EMT-type model (Fig. 11b).

C. Simulation Verification - Hybrid MMC

In this section, the MMC model assumes 50% half- and 50% full-bridge submodules in each arm, which limits the nominal negative voltage capability of each arm to 750 V whereas the nominal positive voltage capability remains 1500 V.

1) Comparison of detailed model with EMT-type models: As expected from the results in Section IV-B, the waveforms of the EMT-type models closely match those of the detailed model except for Cases (I) and (IV), where the nominal arm voltage limit is reached (Fig. 7). The dc-side fault current waveform exhibits a longer decay compared with the full-bridge case of Fig. 6a, as the negative voltage capability is reduced. Again, the close match between the EMT-type models and the detailed simulation model supports the assumptions made in Section III-A.

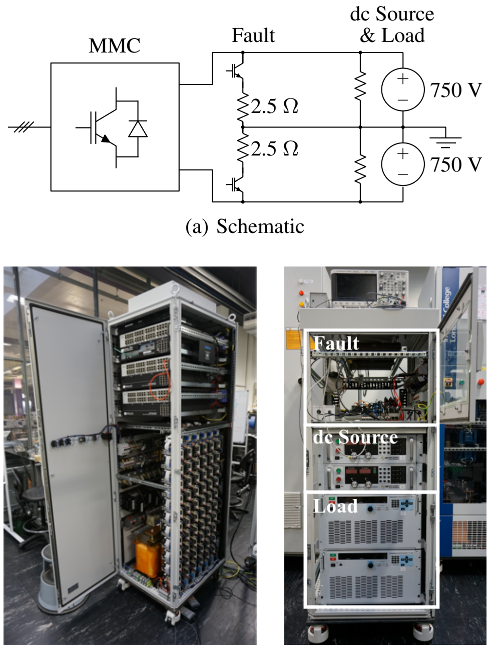
The effect of submodule capacitor charging is more pronounced in the hybrid MMC, and causes the current waveforms produced by the three-phase EMT-type and detailed model to differ fom the full-bridge MMC. The effect is most noticeable in Cases (I) and (IV). In Case (I), the dc-side voltage as requested by the voltage control is the largest of all cases because the pre-fault dc-side current and the dc-side fault current are of the same polarity. For the detailed simulation, the sum of the arm submodule voltages increases beyond the nominal arm voltage limit, which causes the dc-side current to decay faster for the detailed model than for the EMT-type model which does not capture this voltage increase. There are important differences in response between Case (III), in which the converter absorbs reactive power from the grid, and (IV), in which the converter injects reactive power into the grid. In Case (IV), the nominal arm voltage limits are reached for a longer period of time compared with Case (III) because the converter must generate a larger ac-side voltage to inject rather than to absorb reactive power. It was observed that the current waveform produced by the three-phase EMT-type model in Case (IV) decays faster compared with the detailed model (Fig. 7d), in contrast to what occurs in Cases (I) and (III). In Case (IV), the negative voltage injected by the detailed model is initially lower in comparison to that of the three-phase EMT-type model. It should be noted that, in all cases investigated, there was no pattern observed which indicated persistent under- or overestimation of the fault current.

The dc EMT-type model shows a faster decay of fault current compared with the detailed model since it overestimates the available negative voltage capability. The available negative voltage capability depends on the pre-fault arm voltage at the moment of fault inception, and, as a consequence, differs for each of the converter legs.

2) Assessment of influential parameters on model accuracy: The relative performance of the proposed models was tested for the same parameters as in Section IV-B4, i.e., control and sensor delay, and current control proportional gain. The conclusions of Section IV-B4 hold for the greater part of the analysis, except that the waveforms generally show a larger deviation compared with those in Section IV-B4 as nominal arm voltage limits are reached in a larger number of cases and for longer durations. The current control gain has less influence on the output waveforms of the hybrid (Fig. 11d) compared with the full-bridge case (Fig. 11b), as, due to the lower negative available voltage capability, the nominal arm voltage limits are hit before the change in current control takes effect.

V. Experimental Verification

A lab-scale MMC, built to the specifications of Table II and described in detail in [44], was used to explore the validity of the proposed reduced models, the assumption on which they are based and the veracity of the detailed model against which they were compared in the preceding Section. The



(a) Schematic

(b) Converter (c) dc source and load

Fig. 12. Experimental set-up of converter, fault and dc source and load.

converter was operated in conjunction with a dc source, a load impedance and a mechanism for creating a near-short circuit on the dc poles, as shown in Fig. 12. The converter was controlled with a discrete-time controller (with a sample step of 100 μs) implemented on a real-time hardware-in-the-loop (HIL) simulator. All controls except for the current control were taken from [44]. The current control was implemented according to Section IV-A2. The sensor delay was estimated as close to zero and the control delay was estimated as 100 μs, i.e., one control time step. The dc-side fault was emulated using a circuit between the positive and negative pole, comprising two IGBTs and four resistors of 5 Ω. A pair of two parallel-connected resistors and an IGBT was placed between each pole and ground, to give an effective pole-to-ground resistance of 2.5 Ω. The IGBTs were gated-on for as long as the fault persists. The dc source and load were formed of pairs of MAGNA-POWER TSD1000-15 and MAGNA-POWER ARx7.5-1000-15+LXI. The pertinent voltages and currents were obtained via sensors connected to the real-time HIL simulator and sampled every 100 μs.

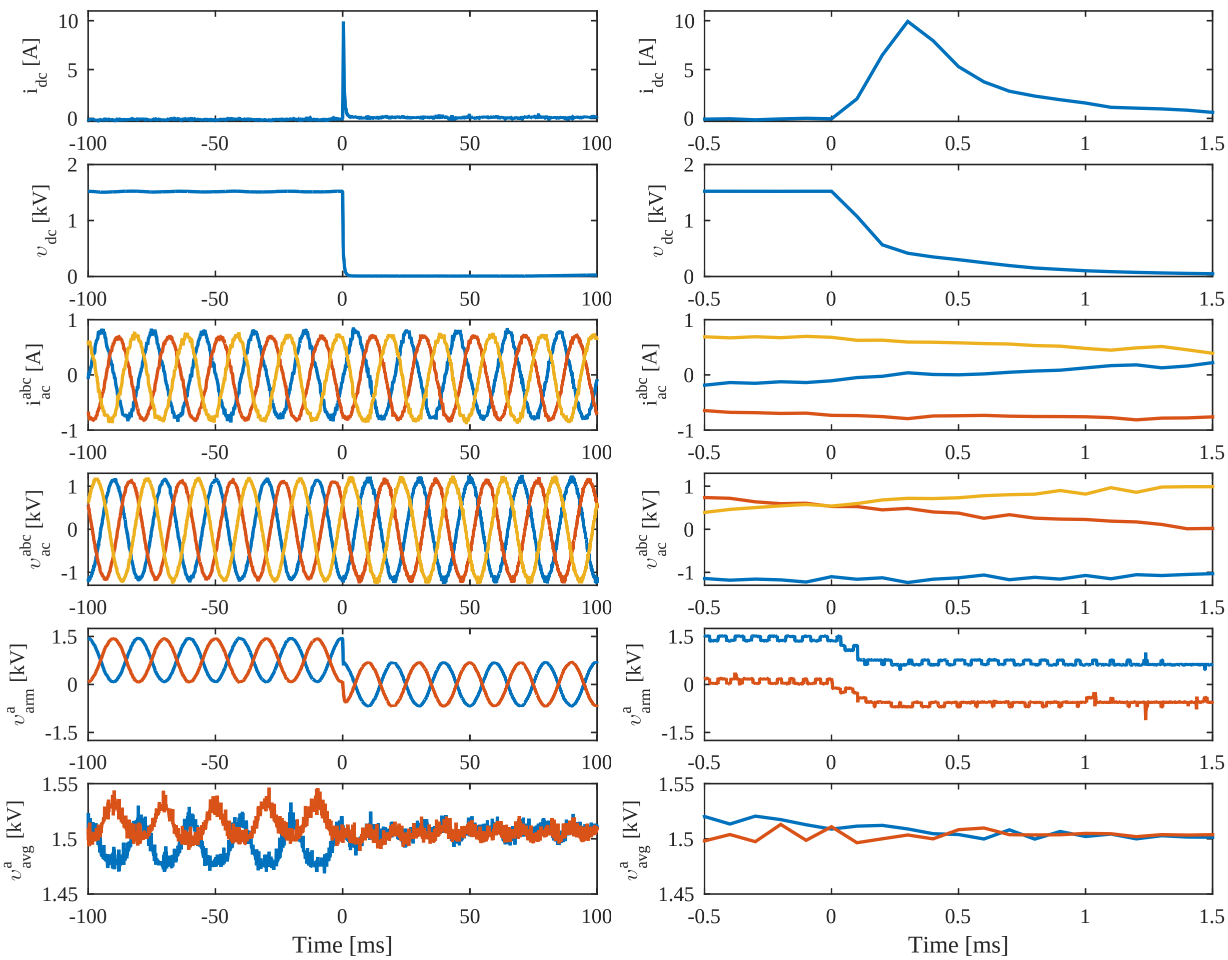
The experiments yielded waveforms with similar shapes as those obtained with the detailed simulation model but give reassurance that the detailed simulation model has not neglected a feature of the system that is relevant to the dc-side fault response. For instance, the waveforms for a dc-side fault under zero load pre-fault conditions obtained with the hardware experiments, shown in Fig. 13, are similar to those of the detailed simulation model, shown in Fig. 5. The difference in peak dc-side fault current (top plots in Fig. 5 and 13), can be attributed to the fact that in the hardware experiments the total delay for the sensors and control is only 100 rather than 200 μs in the simulations. Second, the arm voltages shown by the red and blue lines show a similar overall response compared to the arm voltages of the simulation model. The arm voltages in Fig. 5b are the actual arm voltages as obtained with probe measurements, whereas those in Fig. 5a are reconstructed based on control inputs and the measured dc-side voltage. The probe measurements show that the control response during the experiments is smaller than for the simulations, which reflects that the peak dc-side current is lower. The submodule voltages remain balanced and are controlled within a very narrow range during the dc-side fault and subsequent fault handling process, as was the case for the detailed simulation.

To validate the modeling assumptions and to analyze the accuracy of the reduced three-phase EMT-type model against the experimental results, a detailed comparison of current and arm voltage waveforms is carried out for the following pre-fault power set-points: 0.7 pu and -1.0 pu active power and 0.5 and -0.5 pu reactive power set-points. The rectifying case is limited to 0.7 pu active power because of a limitation in the dc loads to absorb the power and a safety margin on the peak fault current to avoid overcurrents in the converter arms.

To compare the waveforms obtained with the experiments with those of the simulations, the dc-side voltage measured in the experimental set-up is used as the dc-side voltage applied at the converter terminals in the simulations. The waveforms obtained from the experimental set-up and the simulation models are shown in Fig. 14 and Fig. 15. In the experiments, the dc-side current waveform was obtained via two methods: the lightblue solid line shows the dc-side current as measured directly at the converter terminals through the HIL controller (and therefore sampled at 100 μs). The green solid line shows an estimate for the dc-side current obtained from measuring the arm currents with a high-bandwidth current probe (the measured upper and lower arm currents are summed up and multiplied by a factor $^3/_2$ to obtain an estimate for the dc-side current). The good correspondence between the waveforms obtained by both measurement methods verifies that the sampling step of 10 kHz provides a sufficiently accurate measurement of the dc-side fault current. These two measures of current can be compared to the blue line which is the sampled-time result for dc-side current from the simulation of the reduced model. A similar comparison can be made for the arm voltages in Fig. 15 between experimental results in yellow and purple compared with simulation results in blue and red. These results also confirm the expectations on model accuracy obtained from the analysis in Section IV-B.

VI. Conclusion

The dc-side fault response of MMCs with the ability of retaining current control during dc-side faults (i.e., with controlled dc-side fault blocking capability) is primarily determined by the current control dynamics, control and sensor delays, and the degree of negative voltage capability provided by the converter arms. The dc-side fault response can be divided into three successive stages: initial uncontrolled fault current increase, controlled fault current decrease and steady state. To efficiently model this response, three models were developed and were named three-phase EMT-type, a dc EMT-type and transfer function model. The proposed models



(a) Overview over 200 ms

(b) Detail over 2 ms

Fig. 13. Experimental results obtained from the lab-scale converter configured as full-bridge MMC, showing (from top to bottom): dc-side current, dc-side voltage, ac-side current, ac-side voltages, phase A upper arm (blue with yellow overlay) and lower arm (red with purple overlay) voltage and phase A average sum submodule voltage for upper (blue) and lower arm (red) for a dc-side fault at t=0 ms.

have lower model complexity compared with the state of the art, principally because internal variables such as submodule voltages, and their associated balancing controls, are excluded. The experiments with a lab-scale converter prototype support the theoretical analysis and show that the reduced model complexity still provides for accurate representation of dc-side current waveforms over the time intervals of interest.

A verification against a detailed circuit model has shown that all three proposed models are able to accurately represent the dc-side fault response in cases where arm voltages are not restricted by limits imposed by the maximum available negative arm voltage. In case a negative arm voltage limit is reached, the dc-side current control is no longer decoupled from the ac-side and internal balancing current controls, and the three-phase EMT-type model outperforms the two other models. In this case, the sole loss of inaccuracy in the three-phase EMT-type model stems from not incorporating the increase of arm voltages beyond the nominal negative arm voltage limit. An assessment of relative performance of the proposed models has shown that this voltage limit becomes more important, and the dc EMT-type and transfer function models perform worse compared with the three-phase EMT-type model, (i) as the negative arm voltage reduces, (ii) as the proportional gain of the current control is increased, (iii) with increasing control and sensor delay, (iv) for pre-fault rectifying rather than inverting power and (v) with injection of reactive power into the ac system prior to and during the fault. In summary, the three models differ in assumptions made and accuracy achieved, ranging from the transfer function to the three-phase EMT-type model as least to most accurate.

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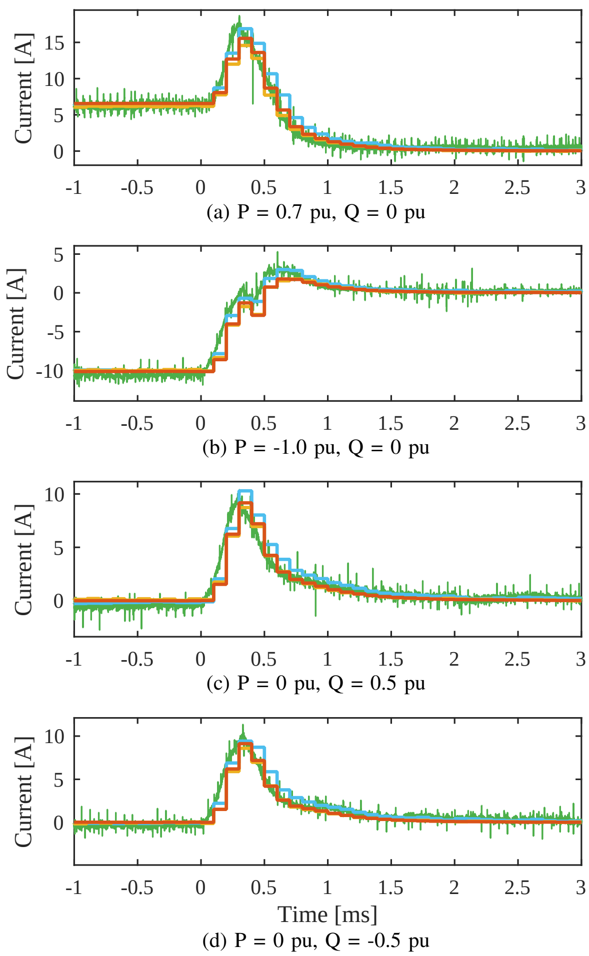

Fig. 14. Comparison of dc-side current waveforms obtained with experimental set-up (solid green and lightblue lines) and detailed (solid yellow line) and three-phase EMT-type (solid red line) simulation model.

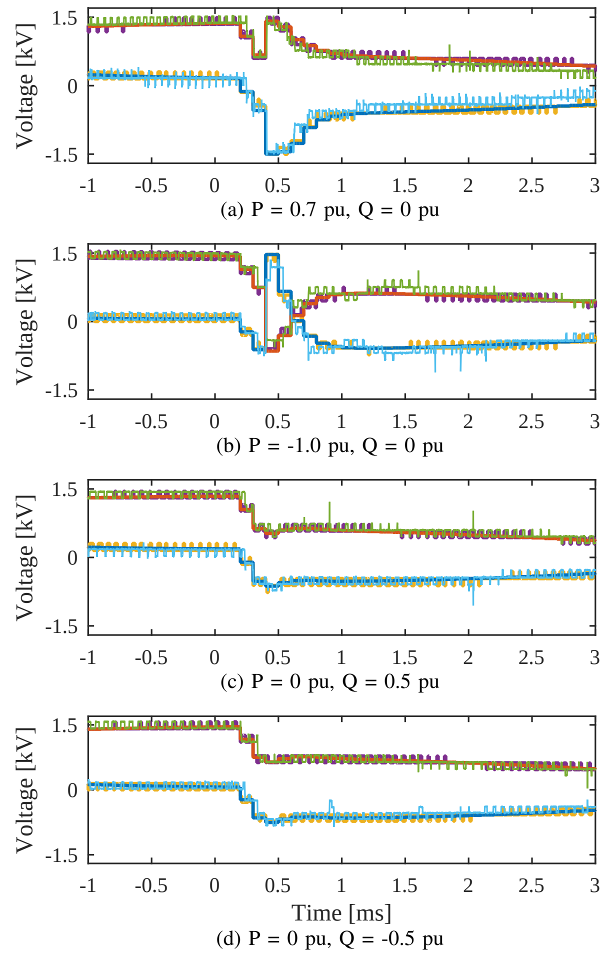

Fig. 15. Comparison of upper and lower arm voltage waveforms for one phase obtained with experimental set-up (solid green and lightblue lines), and detailed (solid purple and yellow lines) and three-phase EMT type simulation models (solid red and blue lines).

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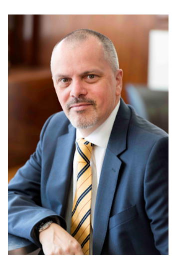

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